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Some design and integration considerations for piezoelectric sensors based on individually contacted vertical ZnO nanowires

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Abstract : We report our last progress about the concept of collecting piezoelectric charges from vertical zinc oxide (ZnO) nanowires (NWs) for development of force-displacement sensor. Finite element (FE) modeling of NW pixels achievable through realistic microfabrication processes showed that piezopotential collection efficiencies of about 60% could be obtained by proper design. ZnO seed-layer thickness is an important parameter. The presence of a gap between NWs and contacting electrodes, which could be caused by process variability, was found to result in a sustainable 30 % drop in piezoelectric signal. Heterogeneous integration issues were also addressed, with selective growth of ZnO NWs as part of the microfabrication process. Arrays of µm-long single NWs with diameters in the 150 nm range were obtained by the hydrothermal method on patterned substrates. These simulation and experimental results are providing useful guidelines for the design and integration of high resolution and high sensitivity NW-based force-displacement sensors.

Keywords: *heterogeneous integration, nanowires, piezoelectricity, zinc oxide, sensor, simulation.*

1. Introduction

One-dimensional nanostructures offer a large range of potential applications in nanoelectronic devices. For instance, ZnO piezoelectric nanowires are promising elements for chip functionality enhancement [1]. In this context we are working on the implementation of ZnO NW arrays (Fig. 1) for high sensitivity and high spatial resolution sensor applications [2]. This paper discusses some aspects of the heterogeneous integration of these NWs within conventionnal silicon technologies.

The device exploits the piezoelectric polarization and the resulting change of the I-V characteristics of a semiconductive ZnO NW under bending. In order to integrate such a device, a certain number of issues must be addressed: (i) define a suitable NW-based "pixel" geometry based on the in-depth understanding of pixel piezoelectric behaviour and on technological considerations, (ii) develop specific microfabrication processes such as seed-layer growth and patterning and (iii) implement controlled NW growth on processed chips as part of the fabrication flow.

On one hand, a simulation study of the full contacted pixel of Fig. 1 was carried out. With heterogeneous integration in view, we analyzed the piezo-response of one pixel as a function of ZnO seed-layer thickness and of contact distance to the NW, in order to evaluate the influence of these parameters and account for process variability. On the other hand, the nature of the seed layer is another tunable parameter. Its impact on NW features (namely average diameter, length and tilt angle) was investigated experimentally. Low temperature processes such as hydrothermal growth [3] are the only ones that enable chip post-processing without damage to the underlying layers. Thus, this technique was used to grow ZnO NWs on different clean-room processed polycrystalline layers, both template-free and patterned into arrays.

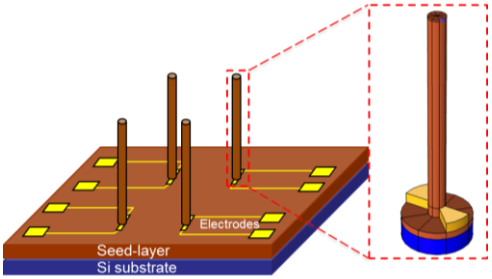


Figure 1: Schematic of the arrayed-NW sensor. Inset: one pixel constituted of an individually contacted vertical NW, with its two electrodes, a ZnO seed-layer (brown) and an Si substrate (blue).

2. Simulation and experimental conditions

A. Finite Element Model

The unit-cell is composed of a 50-nm thick silicon substrate, a piezoelectric ZnO seed-layer of variable thickness, a single vertical piezoelectric ZnO NW (diameter D_{NW}=50nm and length L_{NW}=600nm) and two, 30 nm thick, gold electrodes placed at the NW base, where the piezopotential generated by NW bending is maximum. A clamped edge condition is imposed on the bottom surface of the silicon substrate, and a lateral force of 80nN is applied at the free-end of the NW. Symmetrical contacts were considered. The electrode on the side where the force is applied is grounded, whereas the second one has a floating potential. Simulations were carried out using COMSOL multiphysics®. For the sake of simplicity, and because we were only concerned with general trends, we used linear mechanical parameters and bulk linear piezoelectric coefficients for ZnO. We assumed undoped ZnO with no free charges. The piezopotential attenuation, i.e. the ratio of the piezopotentials in the floating electrode and within the NW, was analyzed as a function of seed-layer thickness (t) and contact to NW distance (d).

B. Nanowire growth

ZnO NWs were synthesized by the hydrothermal method on different ZnO polycrystalline layers. The aqueous solution was prepared with zinc nitrate hexahydrate $Zn(NO_3)_2{\cdot}6H_2O$ and hexamethylene tetramine $(CH_2)_6N_4$ with an equimolar concentration of 30 mM and 10 mM for template-free and patterned substrates, respectively. To promote the growth of nanowires of suitable dimensions, the solutions were heated at 90°C for 16 hours and 5 hours, respectively. For patterned substrates, a triangular lattice of square holes (150 nm × 150 nm with variable spacing) was defined by e-beam lithography and dry-etched through a 100nm-thick SiN_x layer deposited on top of the ZnO seed-layer

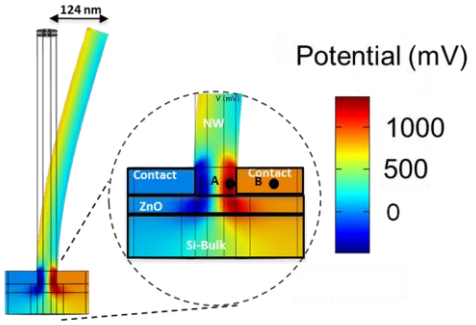
3. Results and Discussion

FEM simulations show that the bottom region of the NW is featuring the highest piezopotential (Fig. 2a). Potential inversion in this region is a known effect due to clamping [4], [5]. A parametric analysis of the seed-layer thickness (t) demonstrated that collection efficiency increases as seed-layer thickness decreases. For a realistic thickness of 20 nm, i.e. a technologically achievable thickness, and for perfect contact between electrode and NW contact (d = 0 nm), piezopotential attenuation was about 60% (Fig. 2b). This value droped to 30% with a few nm gap between contact and NW, and remains quite stable for larger gaps, giving an order of magnitude of what can be expected accounting process variability.

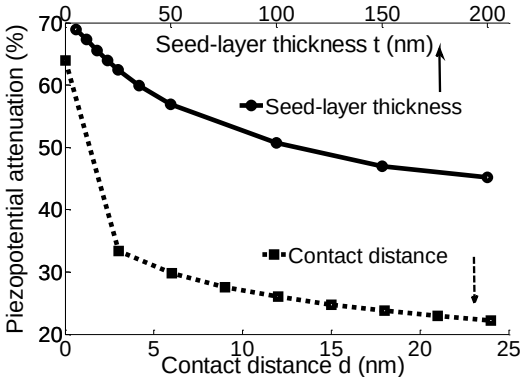
A choice of suitable seed layer of appropriate thickness was then carried out among 13 different cleanroom processed ZnO layers. Deposition techniques included atomic layer deposition (ALD), chemical vapor deposition (CVD) and sputtering. The characteristics of hydrothermally grown ZnO NWs on these layers showed that Gallium-doped ZnO layers deposited at 450°C by CVD yielded low densities of nanowires with targeted dimensions, with µm-long NWs of diameters 85 ± 23 nm and 165 ± 40 nm on template-free and patterned substrates (through 150nm holes spaced by 750nm), respectively (Fig 3a and b). Next steps will include electrode deposition and the characterization of the NW-electrode contact.

4. Conclusion and Perpectives

The simulation results provided insight into device tolerance regarding process variability associated to microfabrication. Regarding heterogeneous integration, a silicon-technology-compatible NW growth process was implemented which yielded controlled-density NW growth on pre-patterned chips, using a low-temperature process that prevents damage of the underlying layers. NW-electrode contacting remains to be validated but these primary results are very encouraging.



(a)



(b)

Figure 2: a) Simulated piezopotential profile within one pixel where points A and B show the maximum potential location within the NW and in the right electrode, respectively; and b) evolution of the piezopotential attenuation as a function of t (full line, d=0nm) and as function of d (dashed line, t=20nm).

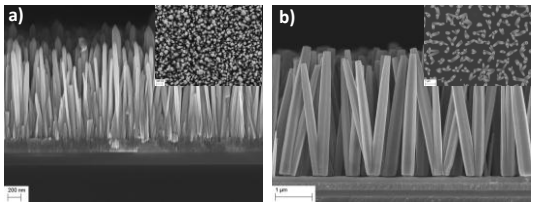


Figure 3: SEM cross-section views of vertical ZnO NWs on Gallium-doped ZnO layers: a) template-free; and b) patterned. The insets are the corresponding top views.

5. Acknowledgments

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6.References:

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